IN THE SPECIFICATION

Please amend the Specification as follows.

Please amend paragraph [0051] as follows:

[0051] By referring to FIG. 1, a reproduced signal waveform processing apparatus according to a first embodiment of the present invention includes: an amplifier 101 for amplifying a reproduced signal 100 obtained from a magnetic medium via a reproducing head; an A/D converter (ADC) 103 for generating a reproduced digital data by sampling the reproduced signal amplified in the amplifier 101; a first equalizer for equalizing the digital data obtained in the A/D converter 103; a second equalizer connected in series with the first equalizer for equalizing an equalized data 303 generated by the first equalizer 301 and inputted thereto; a Viterbi decoder 104 for Viterbi-decoding a reproduced data 107 generated by the second equalizer 302 and for outputting data 109; a phase frequency controller 202 that accepts inputs of the equalized data 303 generated in the first equalizer 301 and a reproducing clock signal 108 for detecting phase frequency error information and outputting a control signal in accordance with a result of the detection; and a voltage controlled oscillator (VCO) 203 for varying its oscillation frequency in response to the control signal from the phase frequency controller 202, and outputting a reproducing clock signal 108. The reproducing clock signal 108 outputted from the voltage controlled oscillator 203 is ~~outputted~~ inputted to the A/D converter 103, the first equalizer 301, the second equalizer 302, the Viterbi decoder 104, the phase frequency controller 202, serving as a synchronizing clock signal for subsequent system stages.

Please amend paragraph [0053] as follows:

[0053] In the reproduced signal waveform processing apparatus having the above-mentioned structure, the reproduced signal 100 obtained from the magnetic medium via the reproducing head is inputted to the A/D converter 103 via the amplifier 101. An output signal from the A/D converter 103 is ~~outputted~~ inputted to the first equalizer 301. Equalized data 303 outputted from the first equalizer 301 is ~~outputted~~ inputted to the second equalizer 302 and to the phase frequency controller 202. An output from the phase frequency controller 202 is ~~outputted~~

inputted to the voltage controlled oscillator 203. The voltage controlled oscillator 203 outputs a reproducing clock signal 108. Reproduced data 107 outputted from the second equalizer 302 is discriminated in the Viterbi decoder 104 and outputted as data 109.